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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: Patwardhan et al.

Attorney Docket No.:  
NSC1P131X3/P04314P03

Application No.: 10/707,208

Examiner: Vikki Trinh

Filed: November 26, 2003

Group: 2814

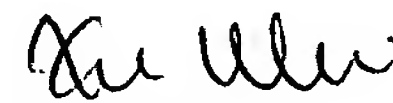
Title: INTEGRATED CIRCUIT DEVICE  
PACKAGE HAVING A SUPPORT COATING  
FOR IMPROVED RELIABILITY DURING  
TEMPERATURE CYCLING

Confirmation No.: 1207

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on July 7, 2005.

Signed: \_\_\_\_\_

  
Susan W. Xu

**INFORMATION DISCLOSURE STATEMENT  
BEFORE FINAL ACTION OR NOTICE OF ALLOWANCE  
(37 CFR §§ 1.56 AND 1.97(c))**

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, copies of non-U.S. Patents are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these citations of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is being filed after the mailing date of the first Office Action on the merits, or after three months of the filing date of this application, whichever event occurred last, but it is believed before the mailing date of either: (i) a final action under

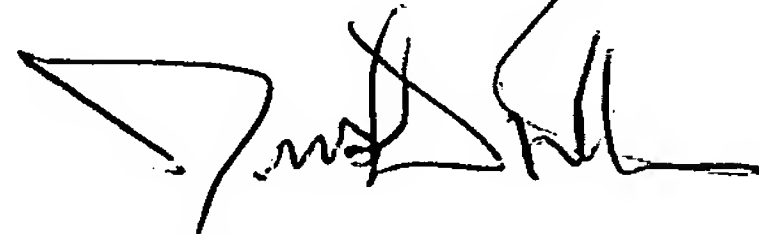
§1.113 or (ii) a notice of allowance under §1.311, whichever occurs first.

Accompanying this Information Disclosure Statement is

☒ the fee set forth in 37 CFR 1.17(p).

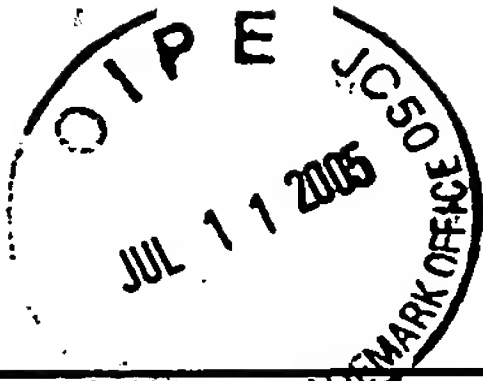
Enclosed is our Check No. 26582 for \$180.00 in payment of the Information Disclosure Statement Fee. If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P131X3).

Respectfully submitted,  
BEYER WEAVER & THOMAS, LLP



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<b>Form 1449 (Modified)</b>  <b>Information Disclosure Statement By Applicant</b>  (Use Several Sheets if Necessary)	Atty Docket No.	Application No.:
	NSC1P131X3/P04314P03	10/707,208
	Applicant:	
	Patwardhan et al.	
	Filing Date	Group
	November 26, 2003	2814

#### U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub- class	Filing Date
	A	6,288,444 B1	09/11/01	Abe et al.			06/04/99
	B						
	C						
	D						
	E						

#### Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub- class	Translation	
							Yes	No
	F							
	G							
	H							

#### Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	I	Kulicke & Soffa, "Flip Chip Products, Polymer Collar™ Wafer Level Package; Achieve Maximum Reliability for Wafer Level Packages!", December 7, 2001, pp. 1-2 <a href="http://www.kns.com">www.kns.com</a>
	J	Kulicke & Soffa, "Flip Chip Division, Polymer Collar Wafer Level Package; See the Polymer Collar WLP difference!", December 7, 2001, pp. 1-2 <a href="http://www.kns.com">www.kns.com</a>
	K	"Fundamentals of Microsystem Packaging", Rao R. Tummala, Chapters 2, 10, and 17, (May 8, 2001) McGraw-Hill Professional Publishing
	L	"Chip Scale Package: Design, Materials, Process, Reliability, and Applications", John H. Lau and S.W. Ricky Lee, Chapter 1, Pages 1-41, (February 28, 1999) McGraw-Hill Professional Publishing
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.